APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

COMPENSATION FOR POLARIZATION MODE DISPERSION IN SINGLE MODE FIBER

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"Express Mail" Mailing Label No. <u>EL875316972US</u>   Date of Deposit *December 21, 2001.*

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COMPENSATION FOR POLARIZATION MODE DISPERSION IN SINGLE MODE FIBER

5 ## BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to detection of data in a communications system, and, more particularly, to compensation for signal dispersion in an optical fiber.

10 Cross-Reference to Related Applications

This application claims the benefit of the filing date of U.S. provisional application no. 60/280,326, filed on 03/30/01 as attorney docket no. Bessios 3PROV.

Description of the Related Art

15 In many digital communications systems, a user generates digital information that is then converted into an encoded (e.g., error-correction encoded) and/or packetized stream of data. The stream of data is then divided into discrete blocks. Each of the blocks may be mapped onto a corresponding one of a sequence of code or symbol values ("symbols") chosen from a pre-defined alphabet A, and generated with a period T_s, sometimes referred to as the "baud" rate. For optical transmission of the digital information,

20 an optical carrier operating with a wavelength of, for example, 1310 nm or 1550 nm, is modulated with the encoded stream of data. The modulated optical carrier is then passed through an optical fiber, such as a single mode fiber (SMF) having its lowest order bound propagating at 1310 nm or 1550 nm.

The modulated optical signal transmitted through the optical fiber comprises a series of light pulses. Since a transmission medium may be modeled as a filter having a corresponding (frequency-

25 domain) transfer function and (time-domain) impulse response, the pulse transmitted through the optical fiber may be modified based on this transfer function. The pulse shape may be modified in amplitude and phase, and also experience dispersion of the pulse. Consequently, the time duration of the pulse transmitted through a medium may extend over a period of time greater than the time duration of a particular symbol. Adjacent pulses transmitted through the medium may thus corrupt each other, which

30 corruption is known as inter-symbol interference (ISI). As bit rates in optical communication systems increase for high speed data transmission, such as rates above 10 Gbps, receivers are increasingly faced

with mitigating effects of pulse dispersion and inter-symbol interference (ISI). A receiver typically includes a detector forming decisions for received, sampled channel output data ("receive signal") corresponding to the transmitted pulses. These detectors may apply compensation/equalization to the input samples of the received signal, and employ algorithms such as maximum-likelihood sequence detection to reconstruct the sequence of pulses in the transmitted, encoded stream of data.

For optical communication systems, there are several sources of pulse dispersion through an SMF. A first source of dispersion is chromatic dispersion that causes time-domain pulse broadening due to the different traveling velocities of each optical pulse's spectral components. Prior art methods of compensation for chromatic dispersion use an opposite dispersion-compensating fiber (DCF) that has a greater dispersion parameter, usually by a factor of 10.

A second source of dispersion is polarization mode dispersion (PMD) that arises from imperfections in the circular symmetry of the fiber core. Imperfections typically are from manufacturing flaws, chemical impurities, and/or excessive bending/ strain during installation. Imperfect circular symmetry results in bi-refringent SMF that causes two orthogonal principal polarization states (PPS) to propagate with different velocities through the fiber core. The average differential group delay (DGD) is proportional to the square-root of the transmission distance. For example, an SMF having PMD of $10ps/\sqrt{L}$, where L is the distance in kilometers, has a DGD of $100ps$ (100 pico-seconds) at a distance of 100km. At distances greater than 100km and bit rates greater than 10 Gbps, the effects of DGD become significant when compared to the symbol period ($T_S=100ps$ at 10 Gbps for non-return-to-zero (NRZ) line coding). For a 10 Gbps transmission data rate, the magnitude of the maximum value for the mean DGD $\langle \tau_d \rangle$ between two orthogonal PPSs has an upper bound of $100ps$ (i.e., $\langle \tau_d \rangle \leq 100ps$).

The (SMF) channel may be modeled as a two-symbol dispersive channel with impulse response $h(t)$, and the model for a 10 Gbps channel that reflects statistical differential delay between the two PPS components may be as given in equation (1):

$$h(t) = \sqrt{\alpha}\left(\delta\left(t - \tau_d\right)\right) + \sqrt{1-\alpha}\left(\delta\left(t\right)\right) \tag{1}$$

with $\delta(\cdot)$ defined as the delta function, with $(\alpha/(1-\alpha))$ defined as the power distribution ratio among the two orthogonal PPSs, and with τ_d following a Maxwell distribution as given in equation (2):

$$P_{(\tau_d)}\left(\tau_d\right) = \frac{32\tau_d^2}{\pi^2 \langle \tau_d \rangle^3} \exp\left(-\frac{4\tau_d^2}{\pi \langle \tau_d \rangle^2}\right) \qquad 0 < \tau_d < \infty \tag{2}$$

ISI results in multi-level channel output values due to the effect of the channel's memory on the binary input levels, causing degradation of a receiver's bit error rate (BER) performance. Linear ISI and time-varying PMD effects are generally compensated by using adaptive equalization.

SUMMARY OF THE INVENTION

The present invention relates to non-linear threshold compensation to adjust input sample values from a single mode fiber to mitigate effects of polarization mode dispersion. In accordance with an exemplary embodiment of the present invention, compensation is applied to samples received from an optical channel by generating a decision for a current sample and a previous sample based on a threshold, and generating a decision difference between the decisions for the current and previous samples as an estimate of the direction ("sign/phase") of decision transition. An error signal is generated as a difference between the current sample and the decision for the current sample; and a sample difference is generated between the current and previous samples. A magnitude of correction is combined with the sign/phase to create a correction value, wherein the magnitude of the correction combined with the sign/phase is selected based on the sample difference, the error signal, and the sign/phase; and the correction value is applied to the current sample to apply compensation.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects, features, and advantages of the present invention will become more fully apparent from the following detailed description, the appended claims, and the accompanying drawings in which:

FIG. 1 shows a block diagram of a decision circuit incorporating non-linear threshold compensation (NLC) in accordance with an exemplary embodiment of the present invention;

FIG. 2 shows graphs illustrating BER performance of a slicer with and without (NLC) in accordance with exemplary embodiments of the present invention given DGD of 70*ps*;

FIG. 3 shows graphs illustrating BER performance of a slicer with and without (NLC) in accordance with exemplary embodiments of the present invention given DGD of 100*ps*;

FIG. 4 shows graphs illustrating noise performance of a slicer with and without NLC in accordance with exemplary embodiments of the present invention given DGD of 100*ps*;

FIG. 5 shows graphs illustrating BER optimization as a function of sampling phase for a slicer with and without NLC in accordance with exemplary embodiments of the present invention;

FIG. 6 shows graphs illustrating BER optimization as a function of threshold for a slicer with and without NLC in accordance with exemplary embodiments of the present invention;

FIG. 7 shows the circuit of FIG. 1 incorporating logic for selecting the magnitude of correction for fixed threshold level;

FIG. 8 shows the circuit of FIG. 1 incorporating logic for selecting the magnitude of correction for adaptive threshold level for first-order symbol transitions; and

FIG. 9 shows the circuit of FIG. 1 incorporating logic for selecting the magnitude of correction for adaptive threshold level for first- and second-order symbol transitions.

DETAILED DESCRIPTION

FIG. 1 shows a block diagram of a decision circuit incorporating non-linear threshold compensation (NLC) in accordance with an exemplary embodiment of the present invention. Circuit 100 includes a first data path having slicer 102; combiner 107 and magnitude operator 108 generating error signal e; a second data path having delay 101 and slicer 103; combiner 104 and magnitude operator 105 generating the signal d; a compensation path having combiner 106, multiplier 109, and combiner 110; and a decision device comprising slicer 111.

The exemplary embodiment of FIG. 1 is described with reference to average differential group delay (DGD) of 100ps and 70ps for data transmitted through a single mode fiber (SMF) with symbol period T_S=100ps at 10 Gbps (with NRZ line coding) and with a channel model as described in equations (1) and (2). In addition, the present invention is described given that, during acquisition, relatively good sampling phase is achieved (i.e., the sampling clock of the received signal generating input samples is relatively close in phase to the phase of the transmitter clock). However, one skilled in the art may readily extend the teachings herein to other optical transmission channels having different differential group delay and different channel models. In addition, the present invention is described for systems with processing with normalized data and sample values. One skilled in the art would realize that the various equations, variables, and thresholds described herein may be scaled or adjusted by constants as determined for a given application.

Non-linear threshold compensation operates as follows. In the first data path, slicer 102 forms a decision for the input sample y_k at time k based on a threshold L. In the second data path, delay 101 delays the input data samples by one sample, and thus, at time k, slicer 103 forms a decision based on a threshold L for the previous sample y_{k-1}. The difference S is generated by combiner 106 as the difference between the

values provided from the first and second paths, which is the difference between i) the decision for the current input sample and ii) the decision for the previous input sample. The value of the difference S indicates whether a transition between logic values has occurred in the input data, and represents the direction (sign/phase) of the transition. An optional divider (not shown in FIG. 1) may be used to divide the value of S by 2 to generate a +1, 0, or -1 value corresponding to the direction of transition. This division by 2 may be desirable if slicers 102 and 103 generate values of +1 or -1 for decisions.

In addition to value S, two values are generated to determine the magnitude c of the correction input to multiplier 109. Combiner 107 and magnitude operator 108 generate a magnitude of an error signal e defined as the magnitude of the difference between i) the decision generated by slicer 102 and ii) the input sample y_k. Combiner 104 and magnitude operator 105 generate the magnitude d of the difference between i) the current input sample and ii) the previous input sample. The value for the difference d represents a relative "closeness" in value between two consecutive input samples.

The magnitude c of a correction combined in multiplier 109 with the sign/phase represented by S is dependent upon the current state of S, e, and d. The magnitude c of the correction for the exemplary embodiment of FIG. 1 may be as given in equation (3):

$$c = \begin{cases} y_k, & \text{if } S < 0, |e| < 0.3 \\ 1 - y_k, & \text{if } S > 0, |e| < 0.3, |d| > 0.13 \\ 0, & \text{Otherwise} \end{cases} \qquad (3)$$

Thresholds for the magnitudes of e and d may be determined experimentally through simulation and observation, such as described subsequently with respect to Table 1.

As shown in equation (3), the decision for which correction to apply is based on detection of the presence or absence of a data transition as indicated by S, closeness in value between two consecutive input samples as indicated by d, and the error between the current sample and the decision for the current sample as indicated by e. When the magnitude c of the correction is combined with S, the result is a correction value that approximates the dispersion effect of the previous data value contained in the current sample. The correction value is then combined with the current sample y_k in combiner 110 to generate a compensated sample. The compensated sample is then applied to slicer 111 that generates a hard decision for the compensated sample at time k. For normalized data, the threshold for slicer 111 is shown as 0.5.

Observation of transmitted data patterns for bit combinations up to three bits through an SMF at 10 Gbps allows for generation of a table of rules for a range (normalized between 0 and 1) of values for the current sample y_k given the previously transmitted data bits. These rules are based on the contributions of previous bit values d_{k-1} and d_{k-2} to the current sample y_k corresponding to the current bit d_k. For receiver 100, Table 1 summarizes an exemplary list of rules. In Table 1 "+" corresponds to a logic "1" transmitted

as a pulse with a given shape, and "-" corresponds to a logic "0" transmitted as a pulse with the inverse of the given shape, and y_k is the input sample corresponding to the last symbol in column 1.

Table 1

Transmitted Data Pattern	Range for y_k with DGD=100ps	Range for y_k with DGD=70ps
+ -	[0.20, 0.35]	[0.20, 0.35]
+ - -	~0.20	[0.00, 0.10]
- - -	[0.00, 0.10]	[0.00. 0.005]
- +	[0.60, 0.75]	[0.55, 0.65]
- + +	[0.90, 1.00]	[0.9, 1.00]
+ + +	[0.95, 1.00]	[0.95, 1.00]

For Table 1, the worst case PMD data with either 70ps or 100ps DGD includes up to a 2-level effect on the current symbol level. Consequently, the threshold levels L of each slicer 102 and 103 in FIG. 1 may be set according to the listed ranges of Table 1. For example, from Table 1 a threshold L for a current decision given the previous sample decision was "+" would be set between the ranges of [0.02, 0.35] and [0.90, 1.00], such as 0.65. As decisions are generated for data, threshold value L may be modified given the decisions for previous samples. In addition, from Table 1 a threshold L for a current decision given the previous sample decision was "-" would be set between the ranges of [0.00, 0.20] and [0.60, 0.75], such as 0.4. Preferred embodiments of the present invention modify L only when a transition between input samples is detected.

FIGs. 2-6 show experimental results comparing the performance of a receiver employing a slicer only to generate decisions for input samples, and a receiver employing non-linear compensation in accordance with embodiments of the present invention. As shown in the figures, employing non-linear threshold compensation in accordance with one or more embodiments of the present invention may improve BER performance, and related SNR performance, of a receiver.

FIG. 2 shows graphs illustrating bit error rate (BER) performance of a slicer with (dashed line) and without (solid line) non-linear threshold compensation (NLC) in accordance with exemplary embodiments of the present invention given DGD of 70ps. As shown in FIGs. 2A-2D, the gain of the slicer with NLC is up to 2 orders of magnitude lower SNR. FIG. 2A is a graph of BER versus signal-to-noise ratio (SNR) for a sampling phase of 5 (SP=5) and threshold L of 0.35. FIG. 2B is a graph of BER versus SNR for a sampling phase of SP=5 and threshold L of 0.25. FIG. 2C is a graph of BER versus SNR for a sampling

phase of 8 (SP=8) and threshold L of 0.35. FIG. 2D is a graph of BER versus SNR for a sampling phase of SP=8 and threshold L of 0.25.

FIG. 3 shows graphs illustrating BER performance of a slicer with (dashed line) and without (solid line) NLC in accordance with exemplary embodiments of the present invention given DGD of 100ps. As shown in FIGs. 3A-3D, the gain of the slicer with NLC is up to 2 orders of magnitude lower SNR. FIG. 3A is a graph of BER versus SNR for a sampling phase of 5 (SP=5) and threshold L of 0.3. FIG. 3B is a graph of BER versus SNR for a sampling phase of SP=5 and threshold L of 0.25. FIG. 3C is a graph of BER versus SNR for a sampling phase of 8 (SP=8) and threshold L of 0.3. FIG. 3D is a graph of BER versus SNR for a sampling phase of SP=8 and threshold L of 0.25.

FIG. 4 shows graphs illustrating noise performance of a slicer with (dashed line) and without (solid line) NLC in accordance with exemplary embodiments of the present invention given DGD of 100ps. FIG. 4A is a graph of BER versus SNR for a simulation with a sampling phase of 5 (SP=5) and threshold L of 0.3, and FIG. 4B is a graph of data value amplitudes versus sp (baud-rate sampling time) without added noise and without compensation. FIG. 4C is a graph of data value amplitudes versus sp (baud-rate sampling time) with added (white Gaussian) noise but without compensation, while FIG. 4DC is a graph of data value amplitudes versus sp (baud-rate sampling time) with added (white Gaussian) noise and with NLC. Comparing FIGs. 4C and 4D illustrates improvement in noise margin when a slicer employs NLC in accordance with an exemplary embodiment of the present invention.

FIG. 5 shows graphs illustrating BER optimization as a function of sampling phase for a slicer with (dashed line) and without (solid line) NLC in accordance with exemplary embodiments of the present invention. FIG. 5A shows BER optimization as a function of sampling phase for an SNR of 25dB and threshold of 0.6 for DGD of 50ps. FIG. 5B shows BER optimization as a function of sampling phase for SNR of 25dB and a threshold of 0.25 for DGD of 70ps. FIG. 5C shows BER optimization as a function of sampling phase for SNR of 25dB and a threshold of 0.35 for DGD of 70ps. FIG. 5D shows BER optimization as a function of sampling phase for SNR of 25dB and a threshold of 0.3 for DGD of 100ps.

FIG. 6 shows graphs illustrating BER optimization as a function of threshold for a slicer with (dashed line) and without (solid line) NLC in accordance with exemplary embodiments of the present invention for sampling phases of 14 (FIG. 6A), 5 (FIG. 6B), 8 (FIG. 6C), and 6 (FIG. 6D).

FIG. 7 shows the circuit of FIG. 1 incorporating logic for selecting the magnitude of correction for fixed threshold level. As shown in FIG. 7, multiplexers (muxes) 702, 703, and 704, and adder 701 implement the tests of equation (3) above. Adder 705 and divider 706 are employed to generate logic 1 or 0 from S for mux 703. FIG. 8 shows the circuit of FIG. 1 incorporating logic for selecting the magnitude

of correction for adaptive threshold level for first-order symbol transitions. The circuit of FIG. 8 is similar to that of FIG. 7 for fixed threshold, except that only one slicer, slicer 102, is used with delay 801 to generate current and previous sample decisions. Slicer 102 employs a threshold $(0.5 + L_1)$, where L_1 is adaptively set based on the combination of 1) the difference between the current and previous output

5   decisions of slicer 102, and 2) a constant l_1 determined from the particular transition from, for example, Table 1. Since only one symbol transition is used, the circuit of FIG. 8 adapts the threshold for first-order symbol transitions (i.e., a current transition from the previous to the current sample including effects of the previous sample). FIG. 9 shows the circuit of FIG. 1 incorporating logic for selecting the magnitude of correction for adaptive threshold level for first- and second-order symbol transitions (i.e., a second order

10   transition is the current transition including effects of both prior symbols). The circuit of FIG. 9 differs from the circuit of FIG. 8 by slicer 102 having its threshold of $(0.5 + L_1 + L_2)$, where L_2 is adaptively set based on 1) the previous difference between output decisions of slicer 102, and 2) constant l_2 determined from the particular transition from, for example, Table 1.

        While the exemplary embodiments of the present invention have been described with respect to

15   processes of circuits, the present invention is not so limited. As would be apparent to one skilled in the art, various functions of circuit elements may also be implemented in the digital domain as processing steps in a software program. Such software may be employed in, for example, a digital signal processor, micro-controller or general purpose computer.

        The present invention can be embodied in the form of methods and apparatuses for practicing

20   those methods. The present invention can also be embodied in the form of program code embodied in tangible media, such as floppy diskettes, CD-ROMs, hard drives, or any other machine-readable storage medium, wherein, when the program code is loaded into and executed by a machine, such as a computer, the machine becomes an apparatus for practicing the invention. The present invention can also be embodied in the form of program code, for example, whether stored in a storage medium, loaded into

25   and/or executed by a machine, or transmitted over some transmission medium, such as over electrical wiring or cabling, through fiber optics, or via electromagnetic radiation, wherein, when the program code is loaded into and executed by a machine, such as a computer, the machine becomes an apparatus for practicing the invention. When implemented on a general-purpose processor, the program code segments combine with the processor to provide a unique device that operates analogously to specific logic circuits.

30   It will be further understood that various changes in the details, materials, and arrangements of the parts which have been described and illustrated in order to explain the nature of this invention may be

made by those skilled in the art without departing from the principle and scope of the invention as expressed in the following claims.